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FIG. 1A

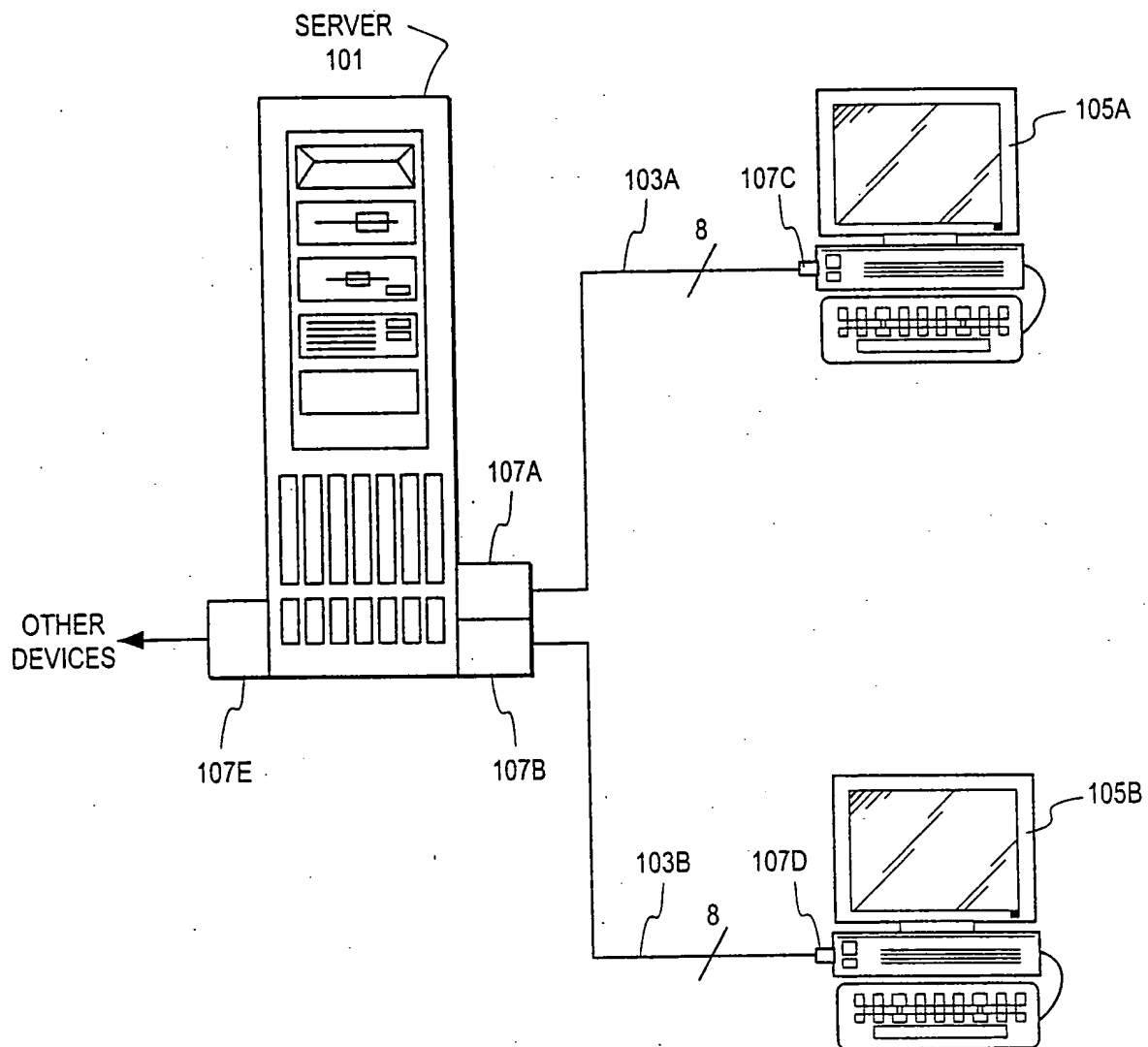
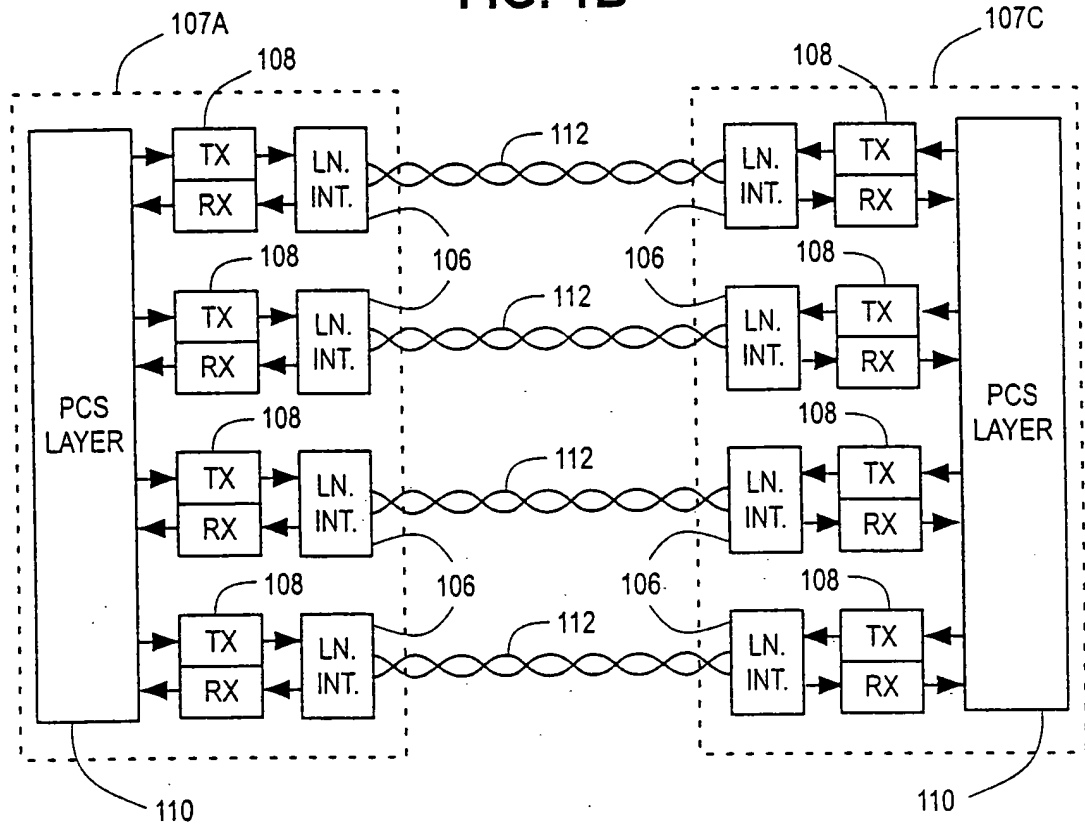


FIG. 1B



200

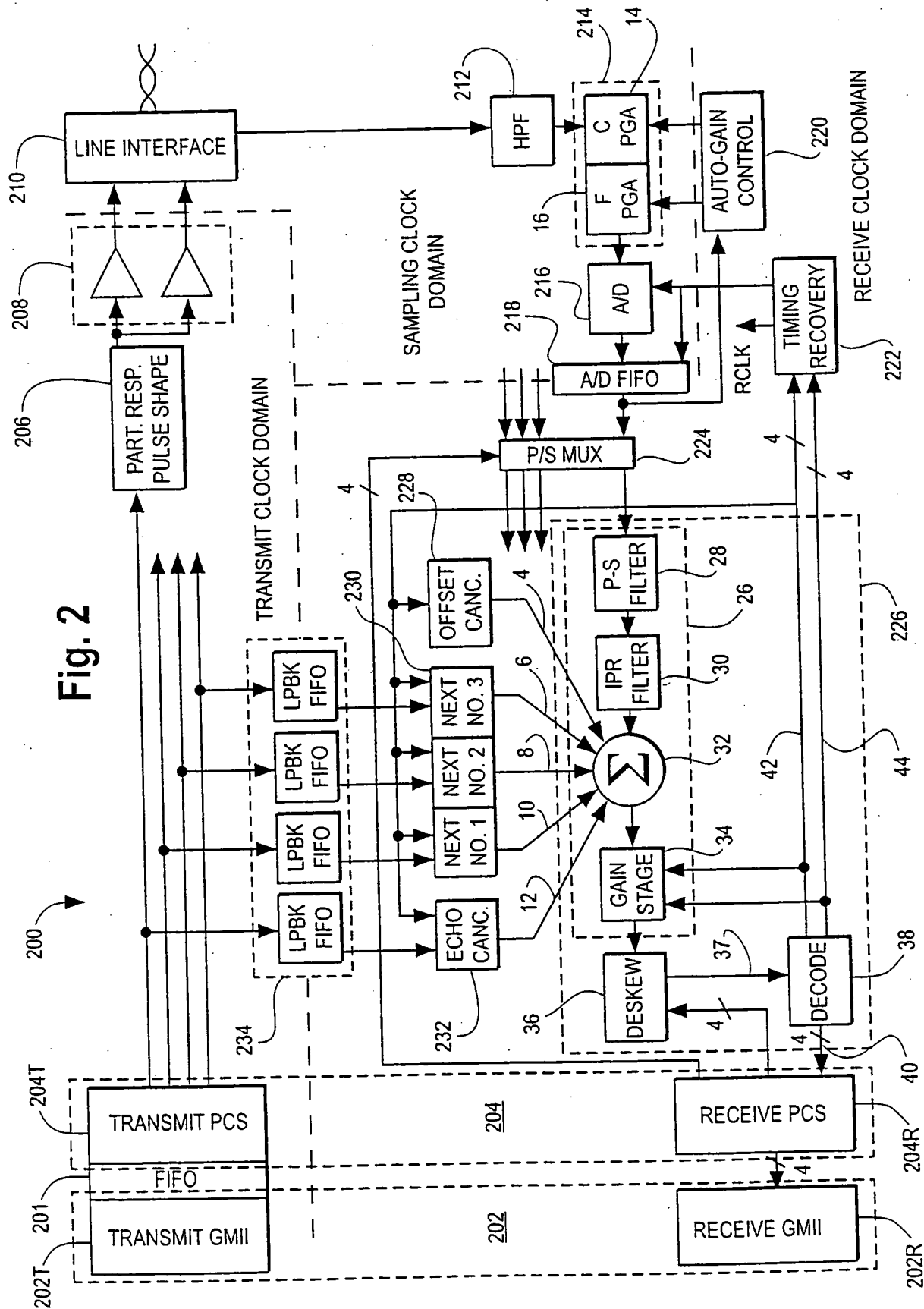


FIG. 3

The block diagram illustrates the control system for the optical fiber sensor. The signal path begins with a **LINE INTERFACE 210**, which is connected to a **HIGH PASS FILTER 212**. The output of the filter is fed into a dashed box labeled **214**, which contains two processing stages: a **COURSE PGA 16** and a **FINE PGA 14**. The output of the fine PGA is then sent to an **A/D 216** converter, followed by an **A/D FIFO 218**. The output of the FIFO is connected to an **AUTOMATIC GAIN CONTROL 220** block. This block provides a **4 BIT** control signal to the **COURSE PGA 16** and a **5 BIT** control signal to the **FINE PGA 14**. Additionally, the **AUTOMATIC GAIN CONTROL 220** receives a **SET POINT** input and a feedback signal from the output of the **A/D FIFO 218**, labeled **222**.

FIG. 4

The circuit diagram, labeled FIG. 4, illustrates a differential signal processing circuit. It features two input buffers, 401 and 403, each receiving an 'IN' signal. The output of buffer 403 is connected to a node that branches into two paths. One path goes through a resistor R 405 to a central node. The other path goes through a resistor R 407 to a node connected to a voltage source V1 (419) and a resistor R 417. This voltage source is labeled VDC=VCM and is connected to ground (GND). Two switches, SW1 (409) and SW2 (411), are connected between the central node and the output nodes of buffers 401 and 403, respectively. The outputs of buffers 401 and 403 are labeled OUT. A second buffer, 413, is connected to the output of buffer 401 and produces a final 'OUT' signal (415).

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FIG. 5

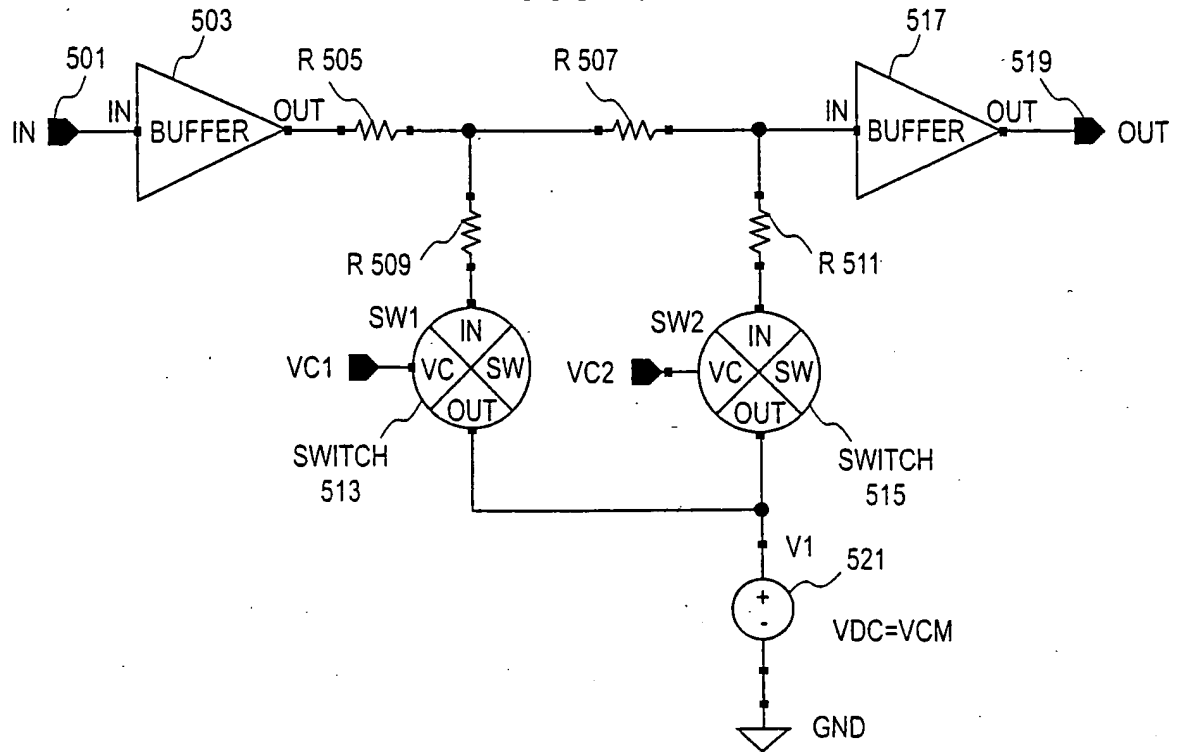


FIG. 6

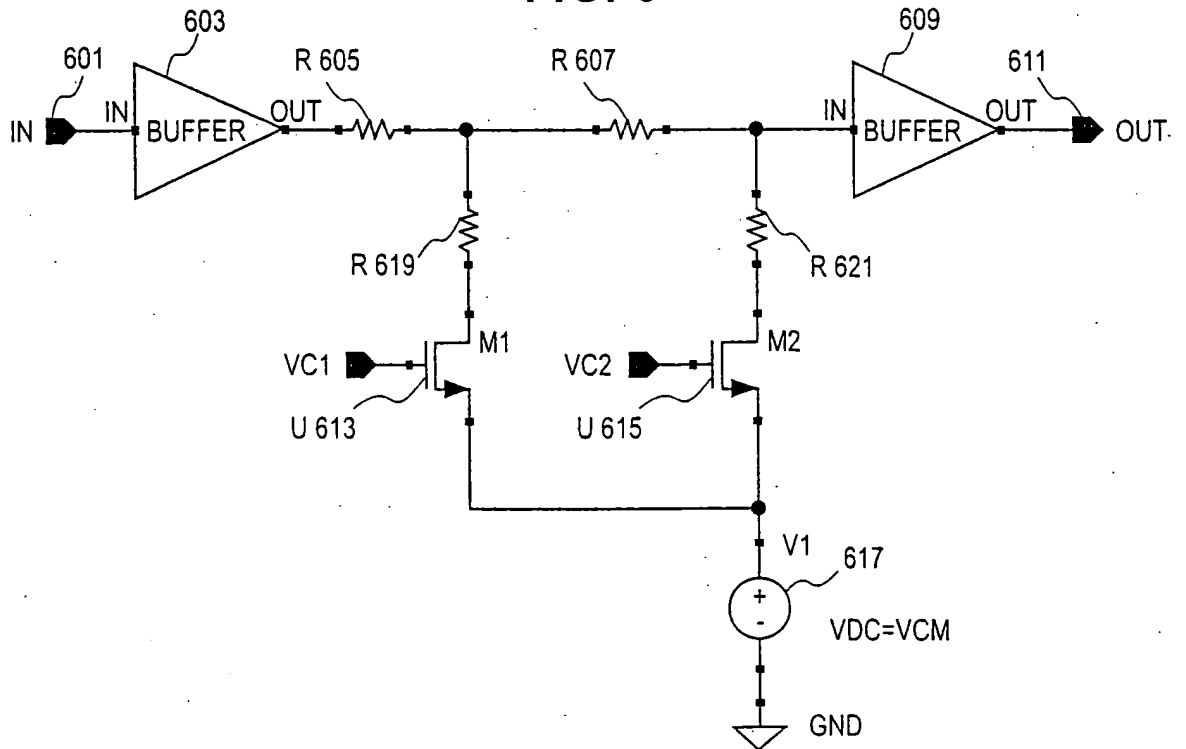
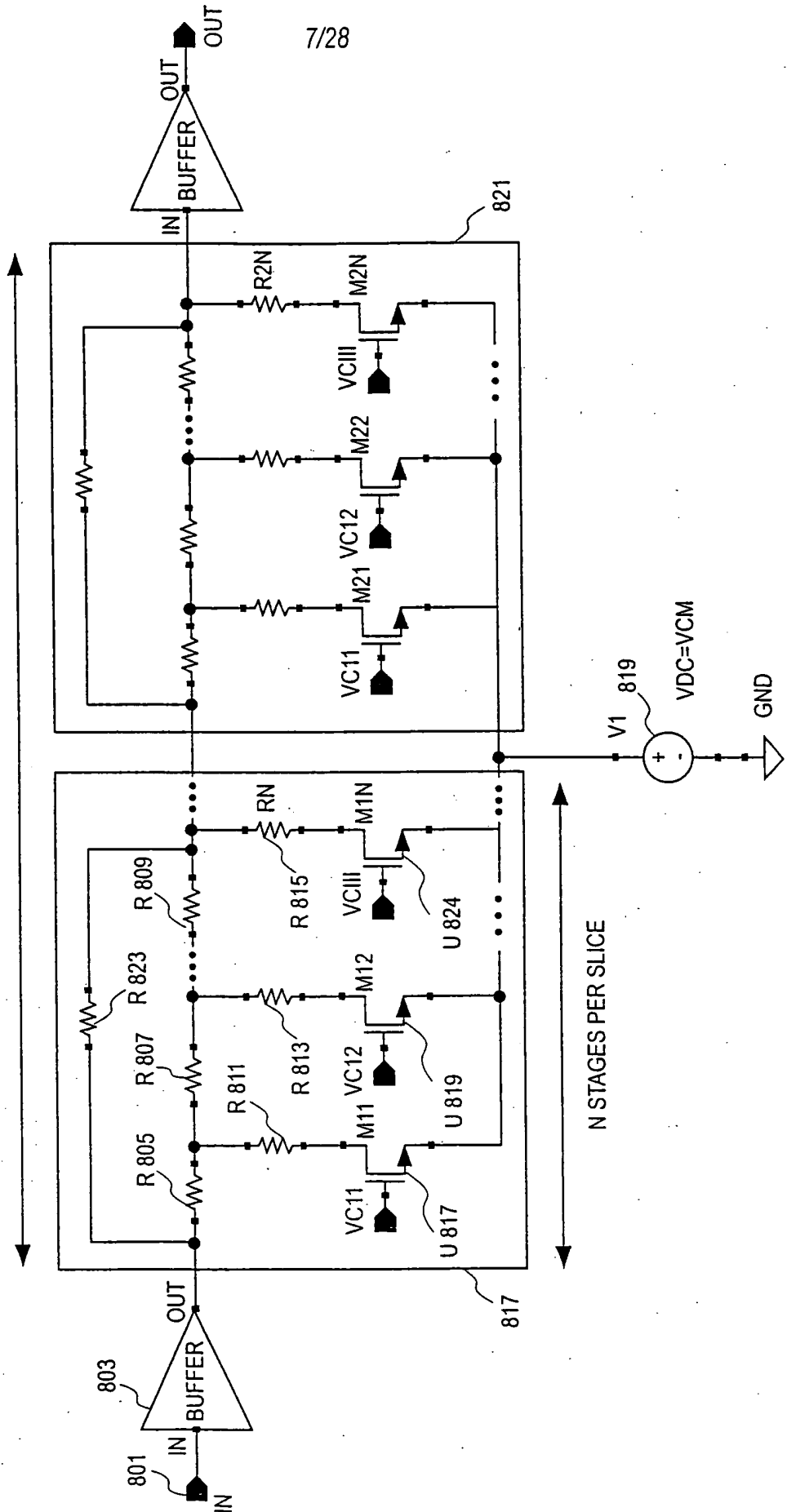


FIG.8

J SLICES



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FIG. 9
 PRIOR ART

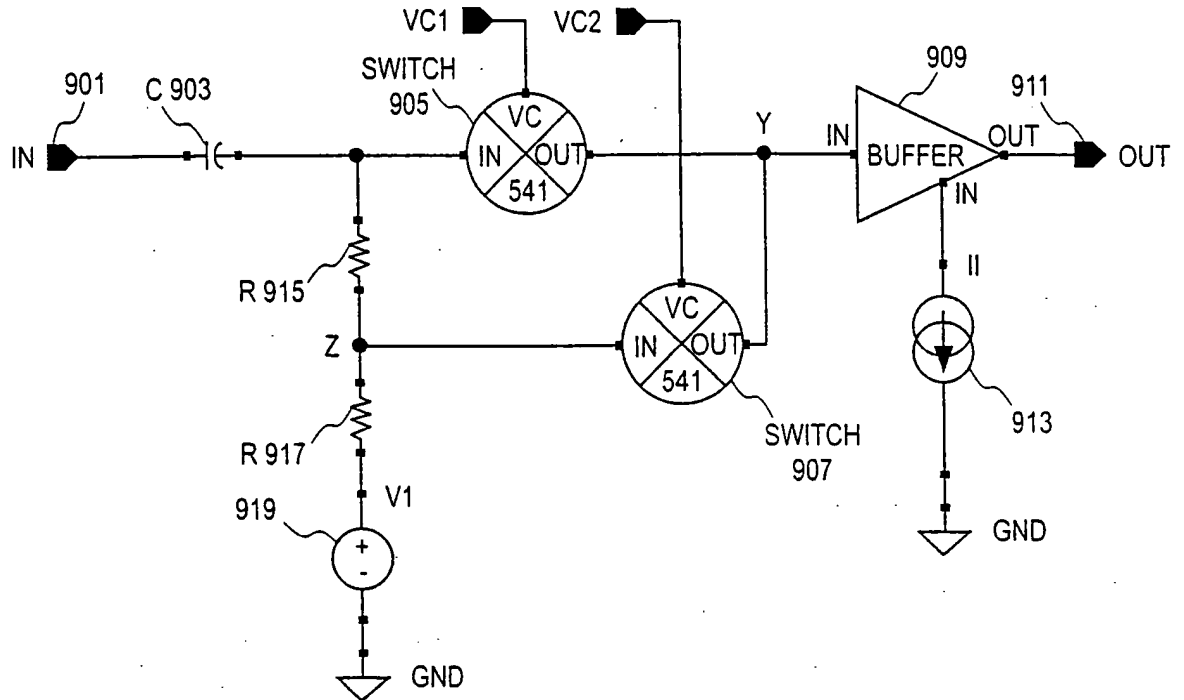
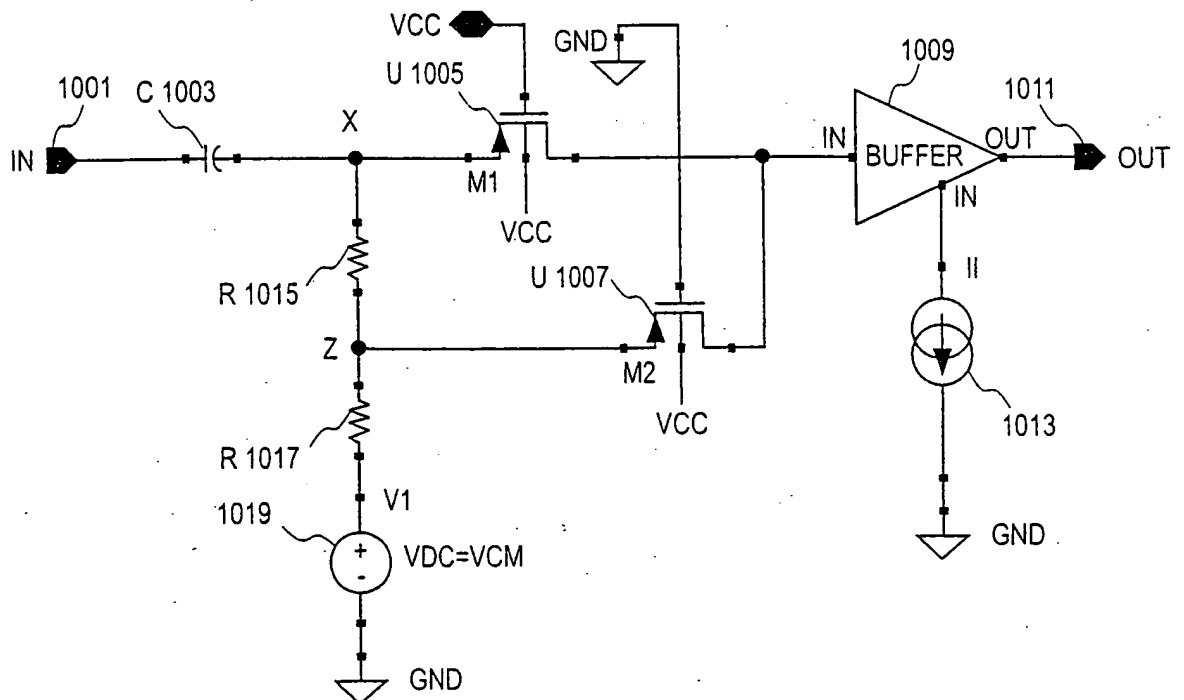
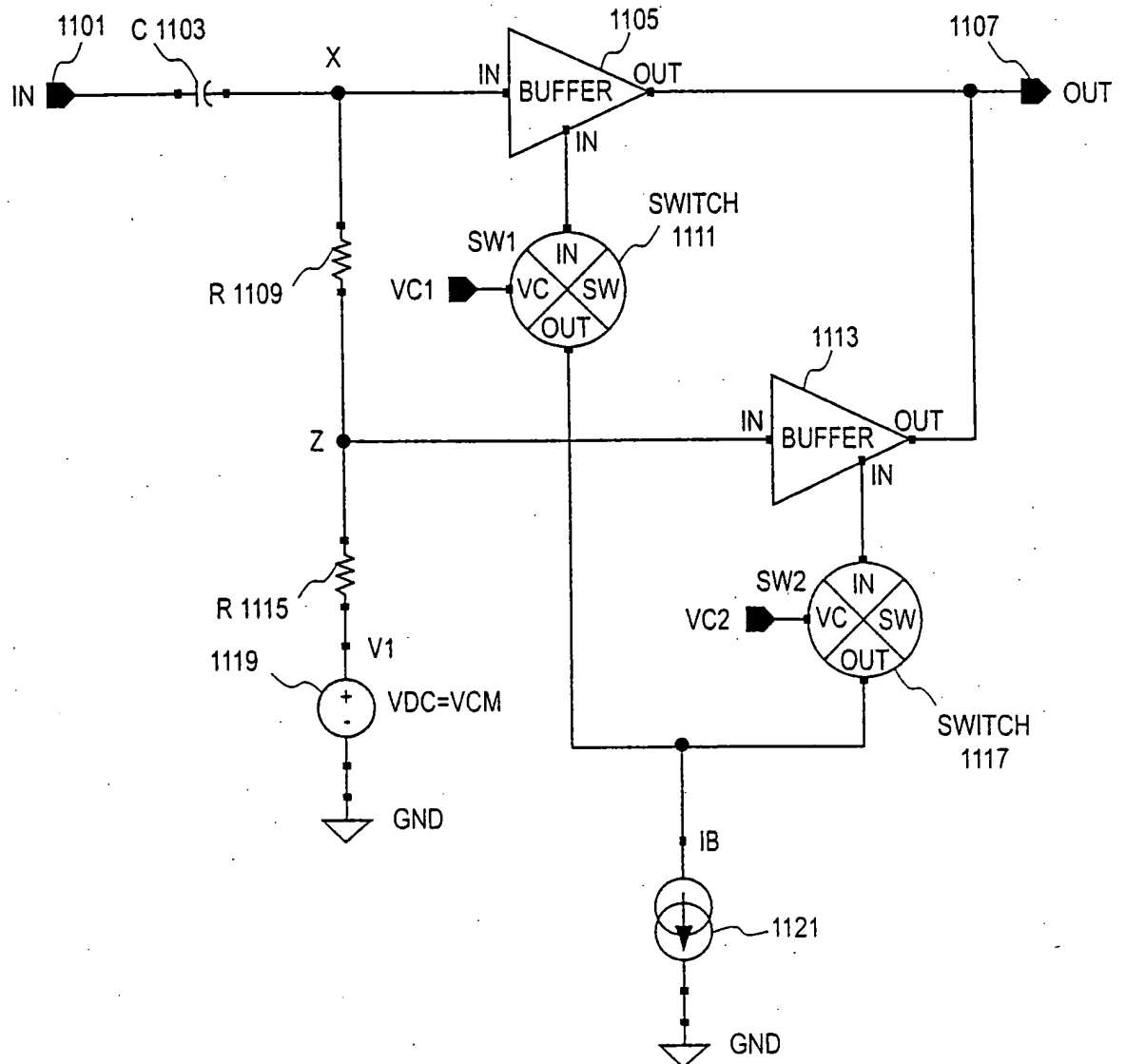


FIG. 10
 PRIOR ART



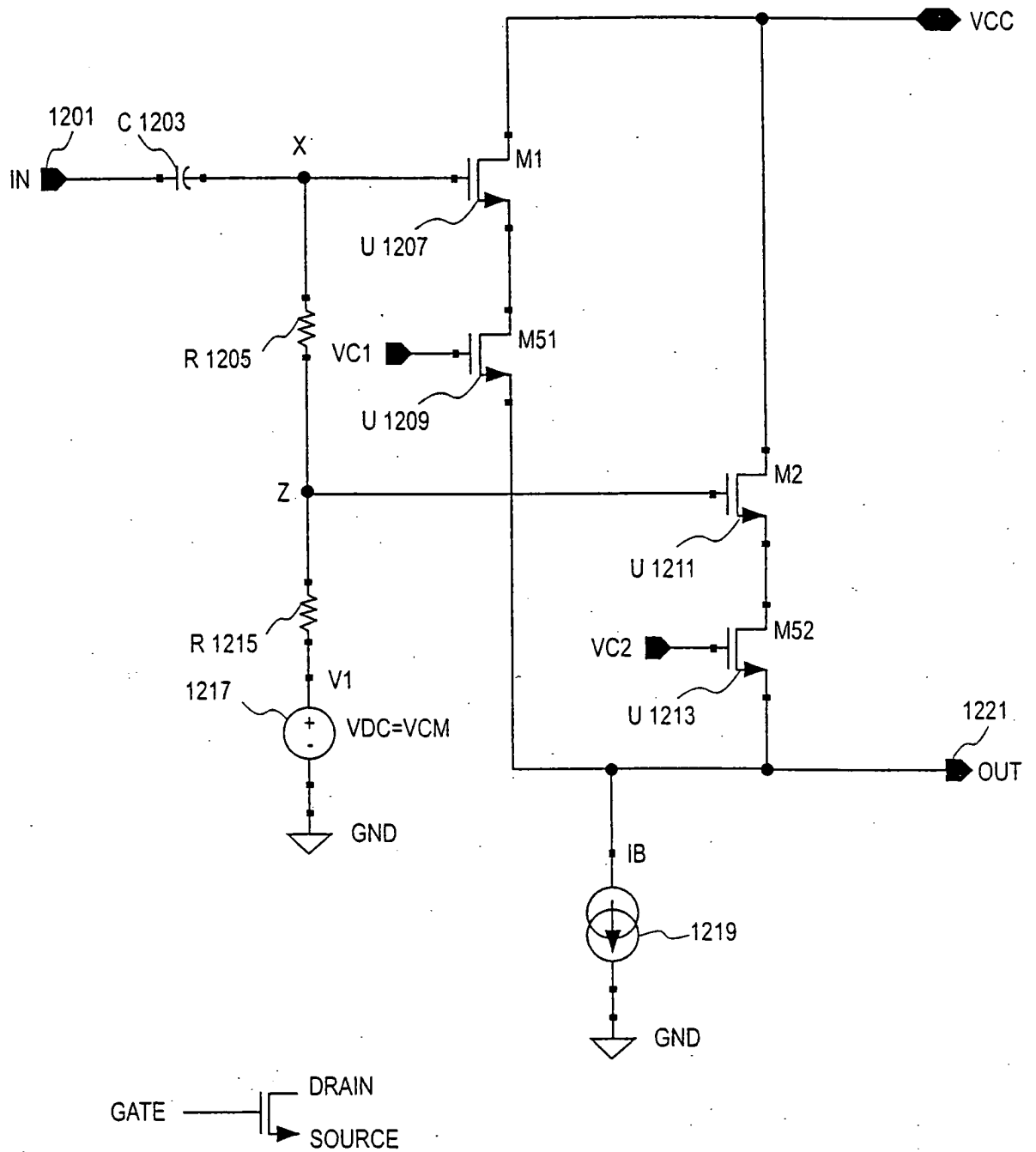
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FIG. 11



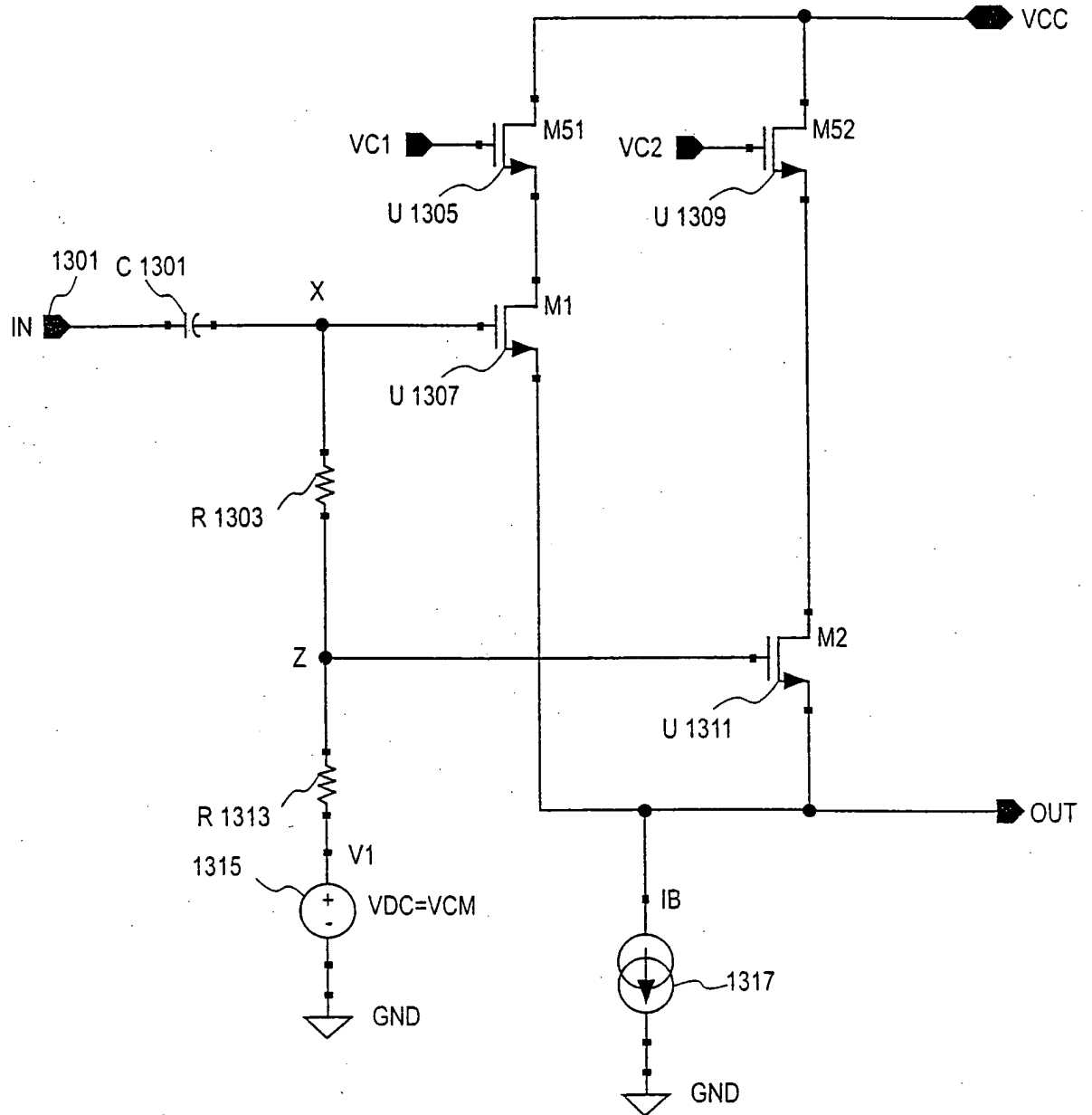
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FIG. 12



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FIG. 13



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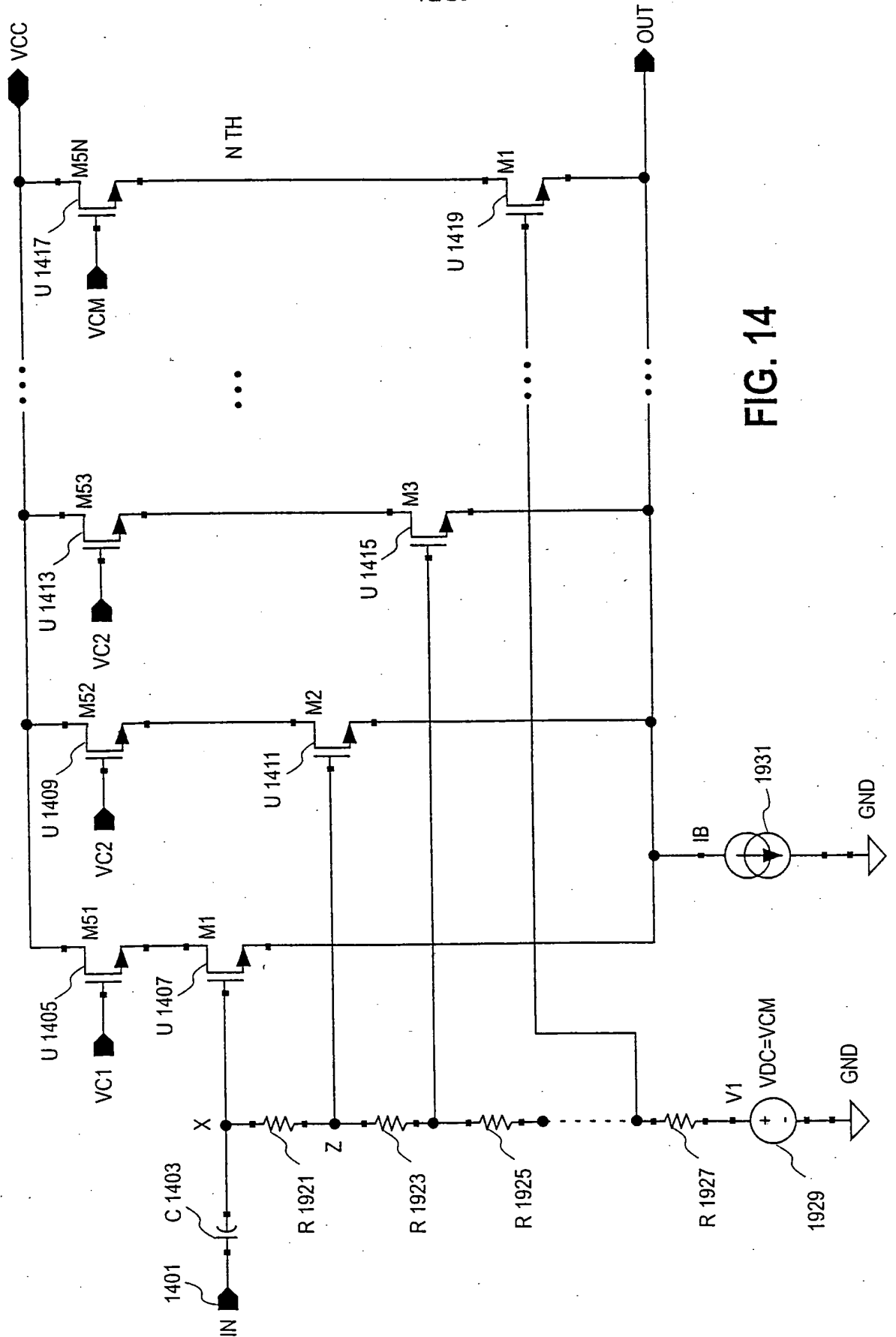


FIG. 14

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FIG. 15

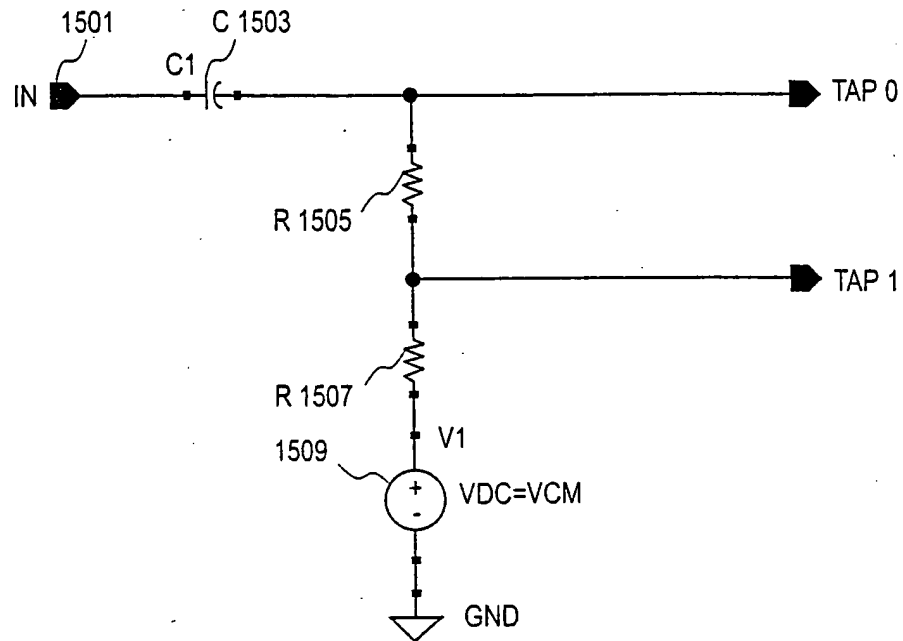
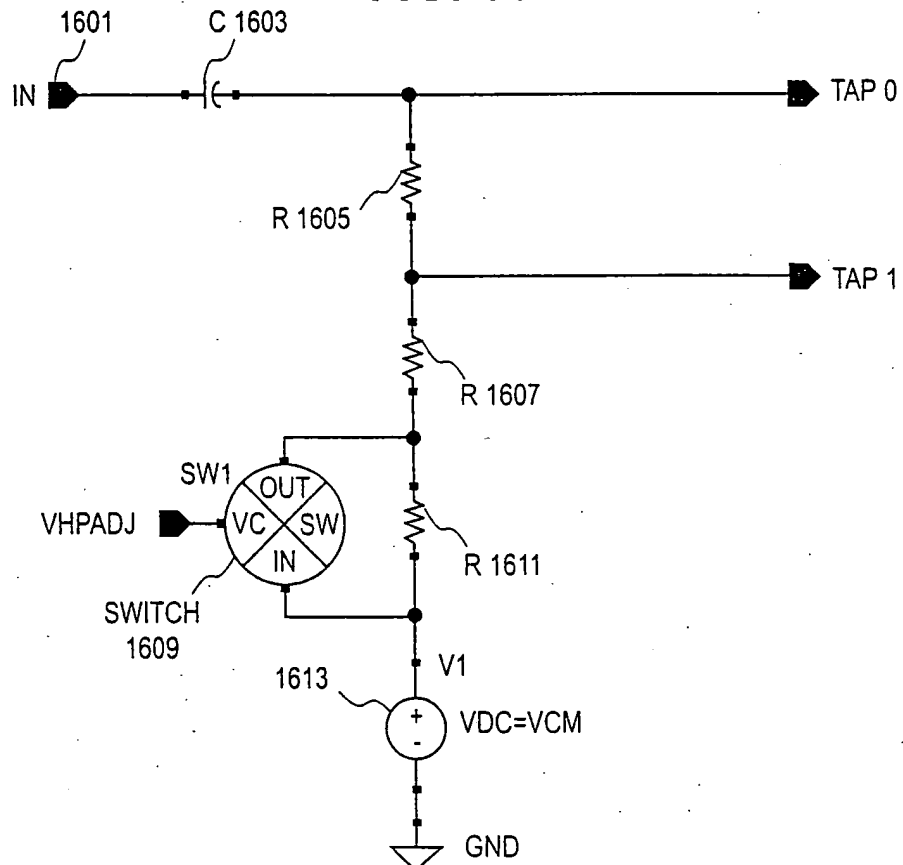


FIG. 16



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FIG. 17

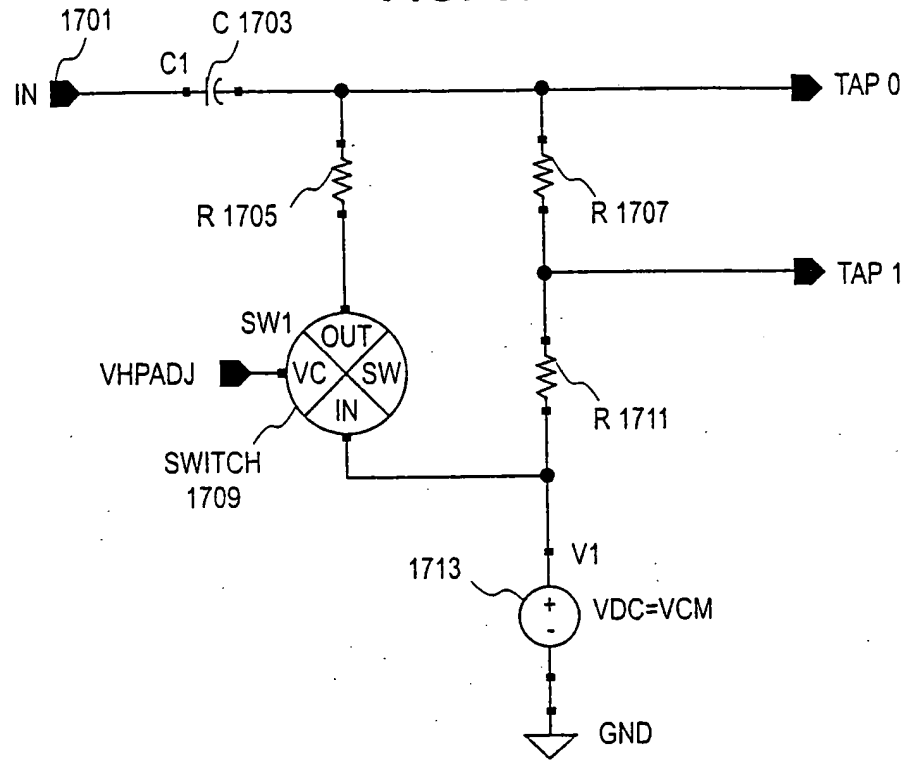


FIG. 18

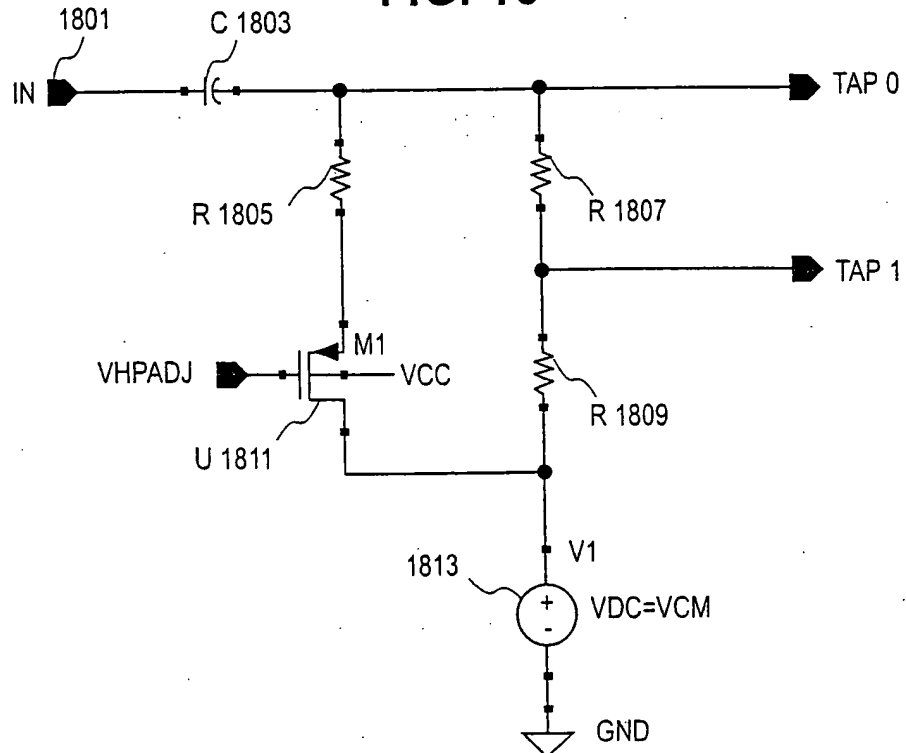


FIG. 19

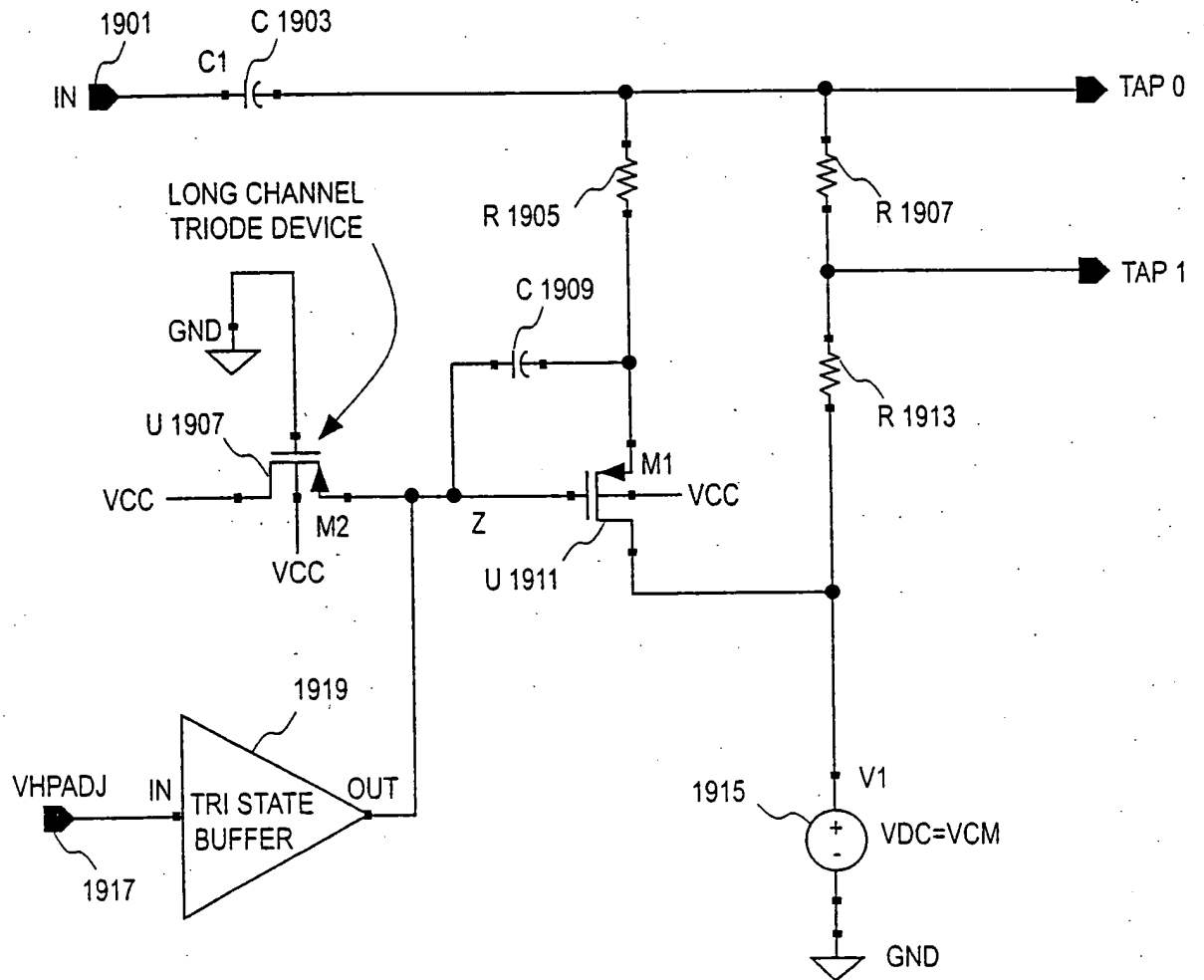
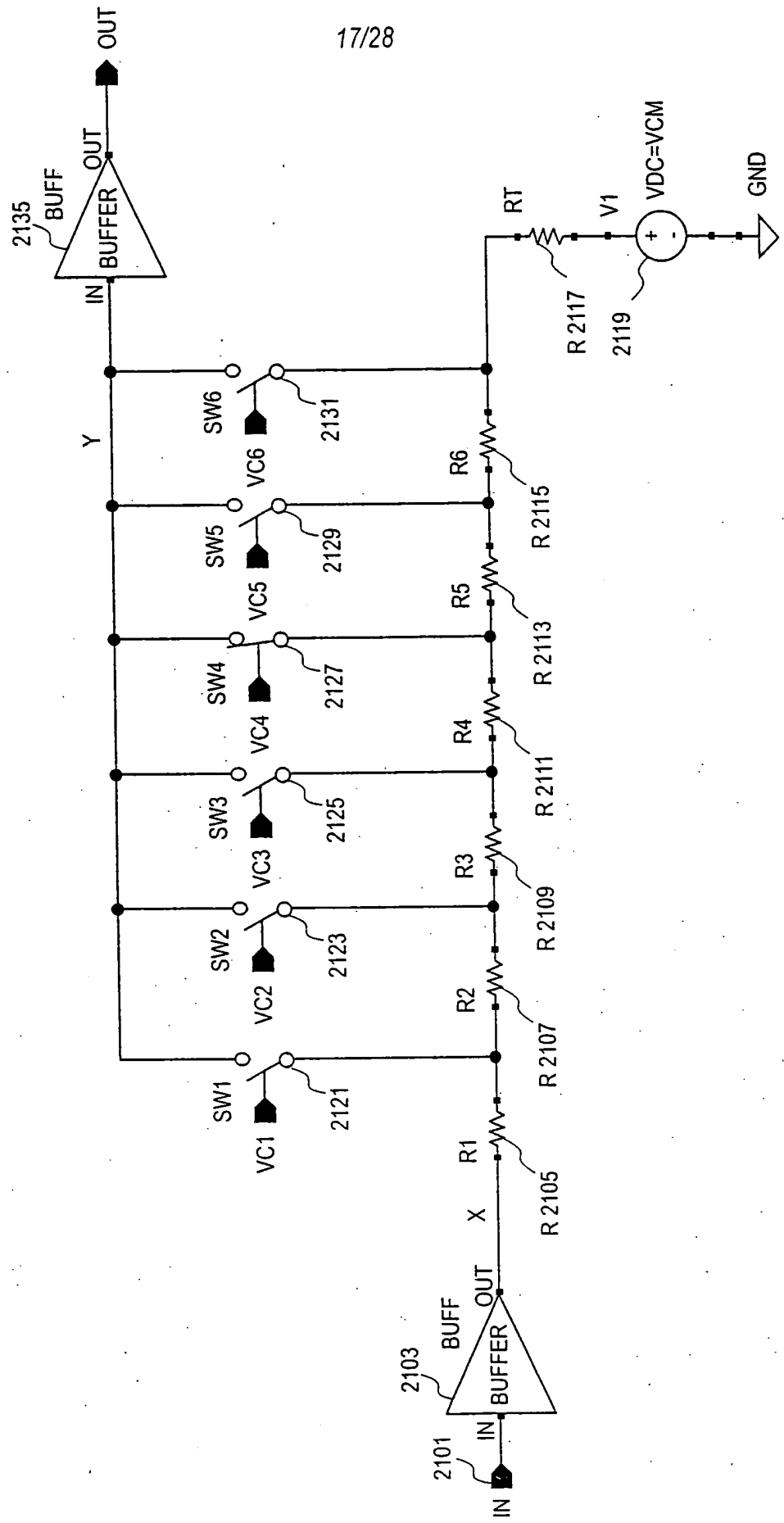
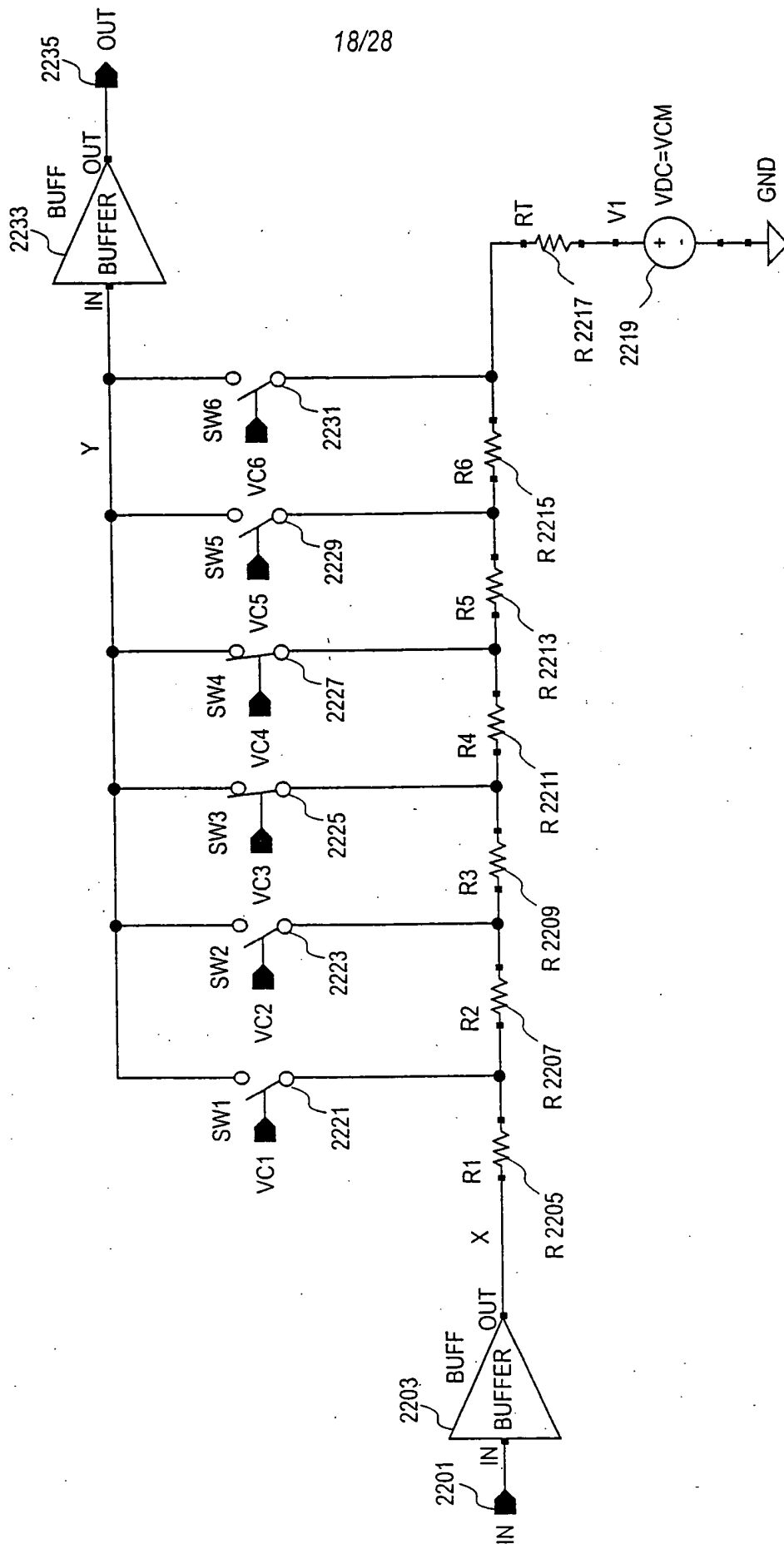


FIG. 21
 PRIOR ART



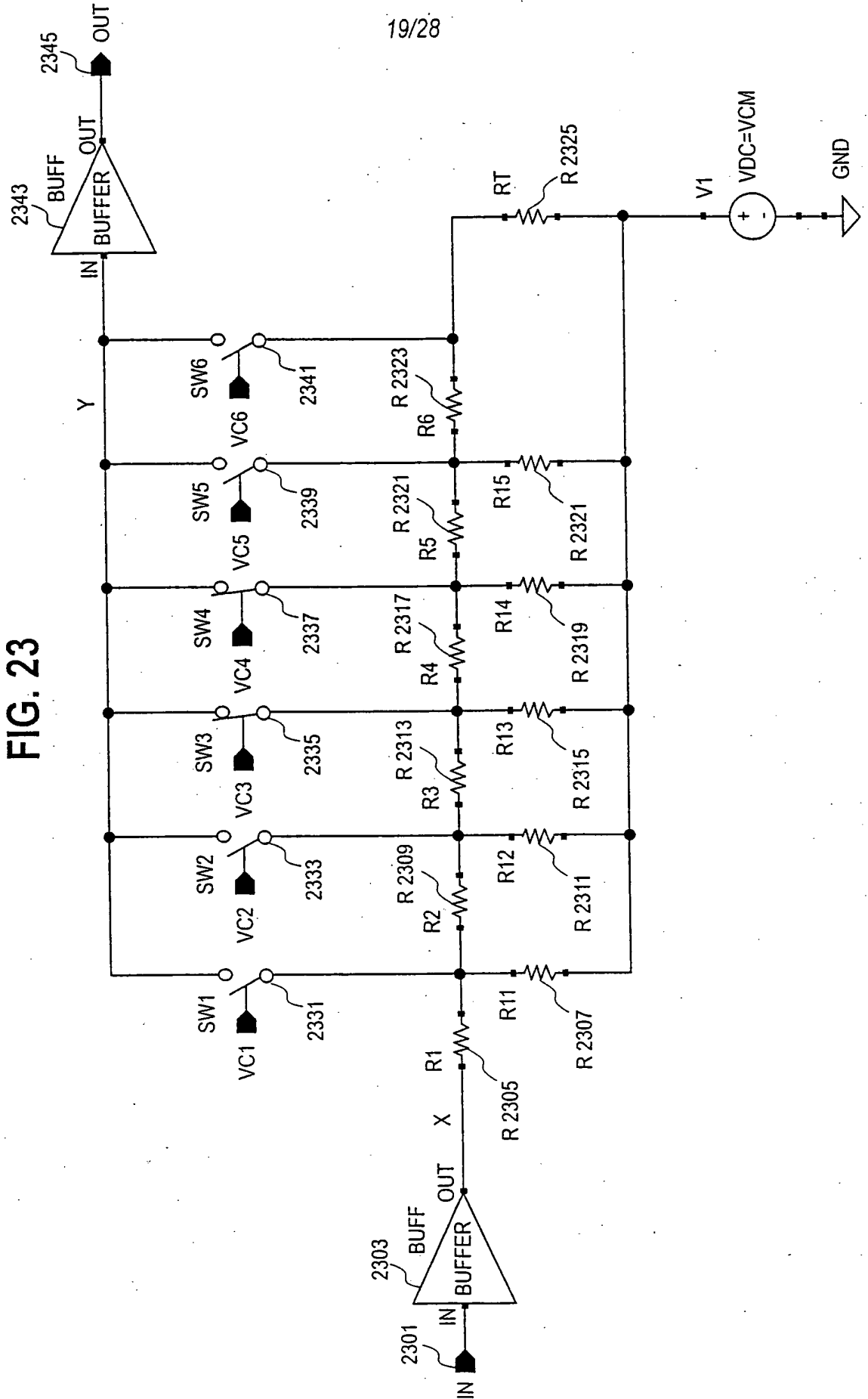
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FIG. 22



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FIG. 23



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FIG. 24

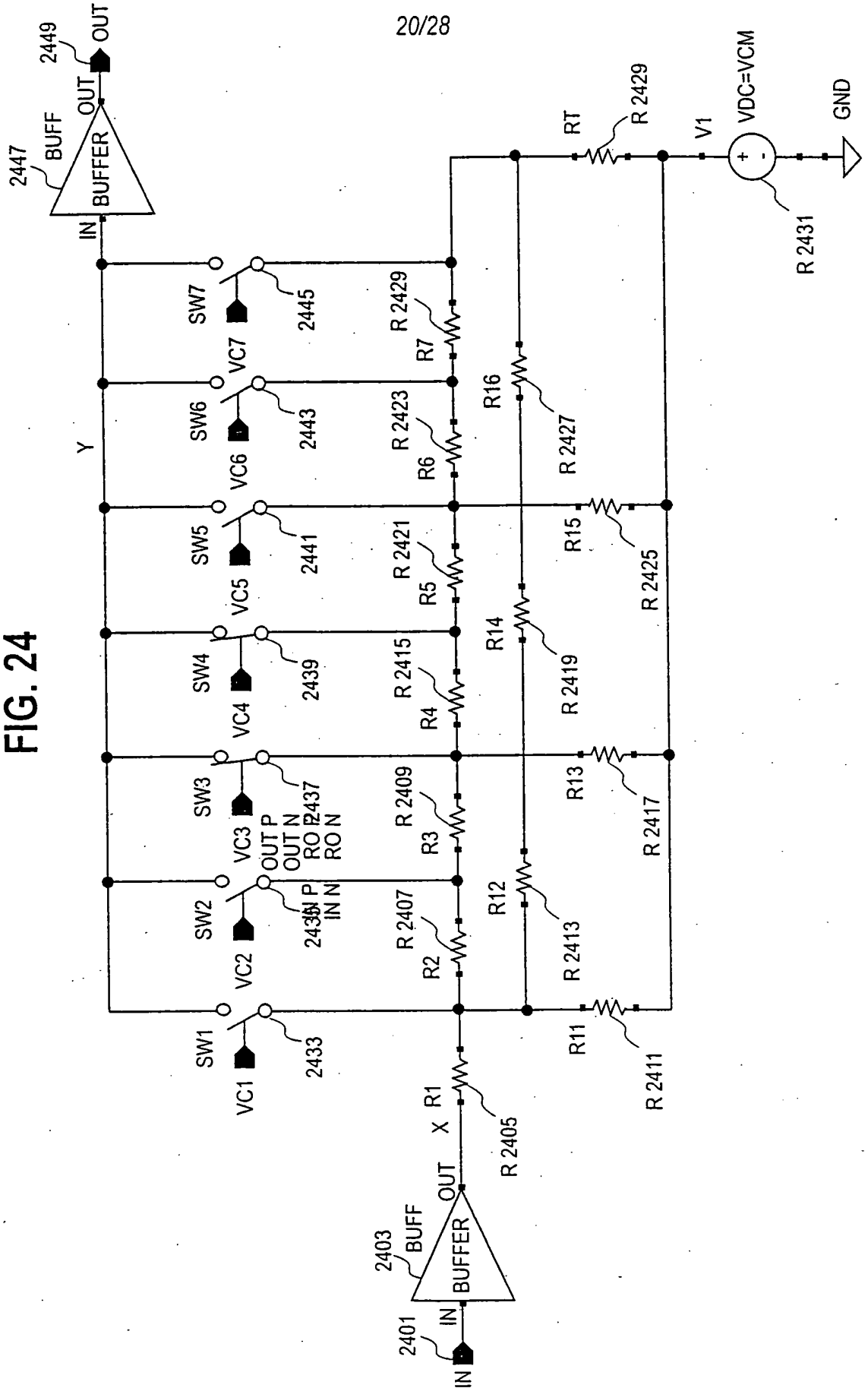
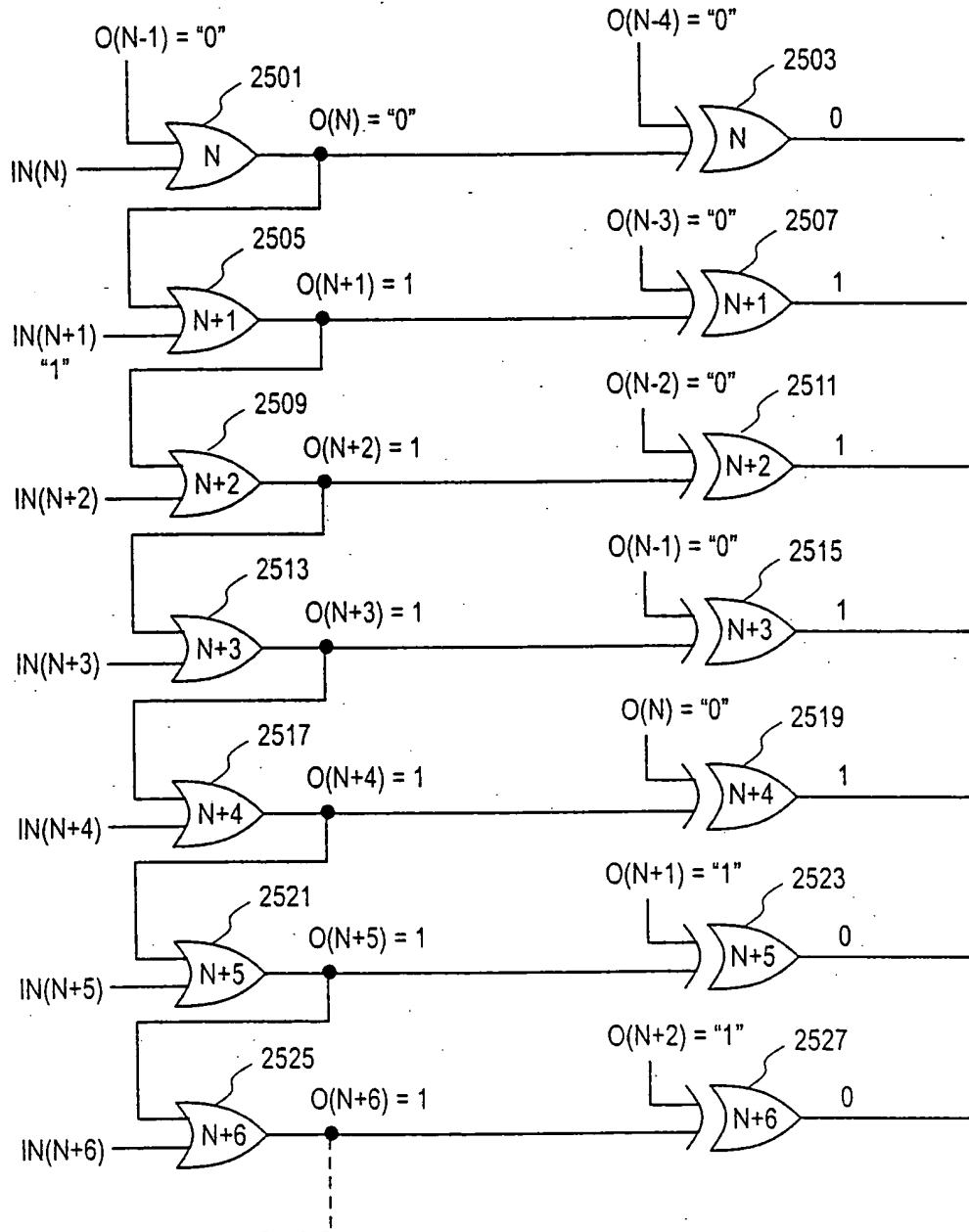


FIG. 25



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FIG. 27

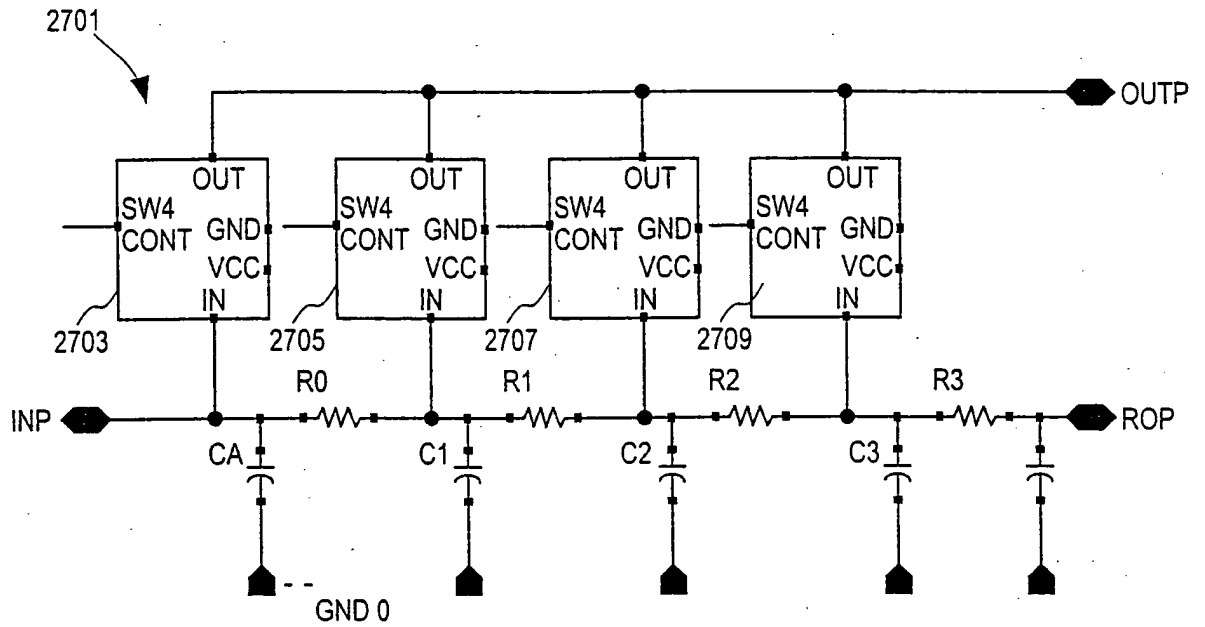
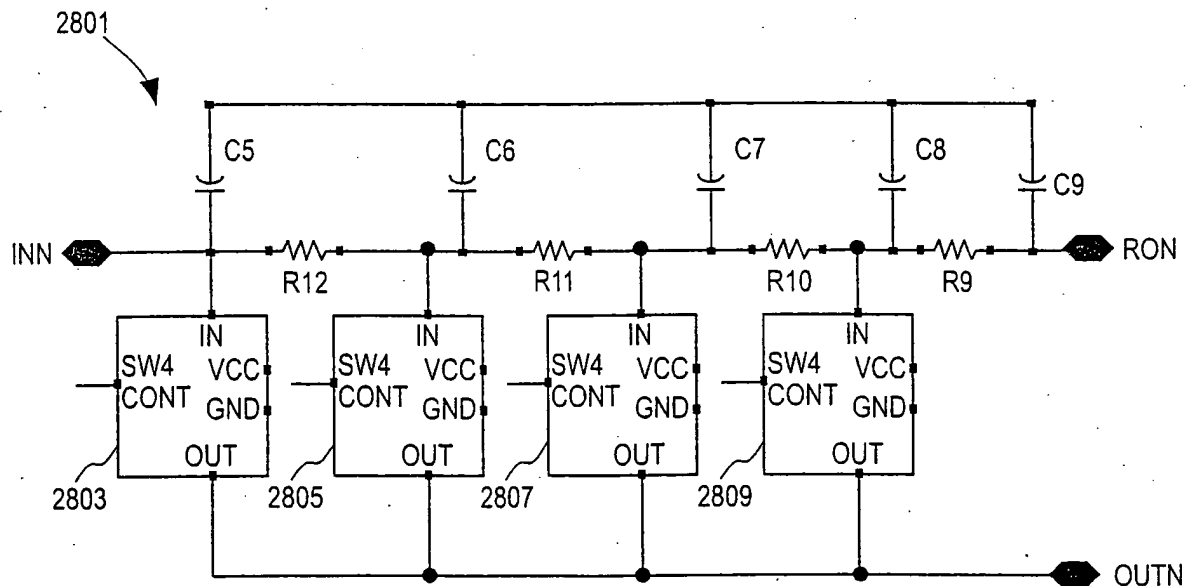
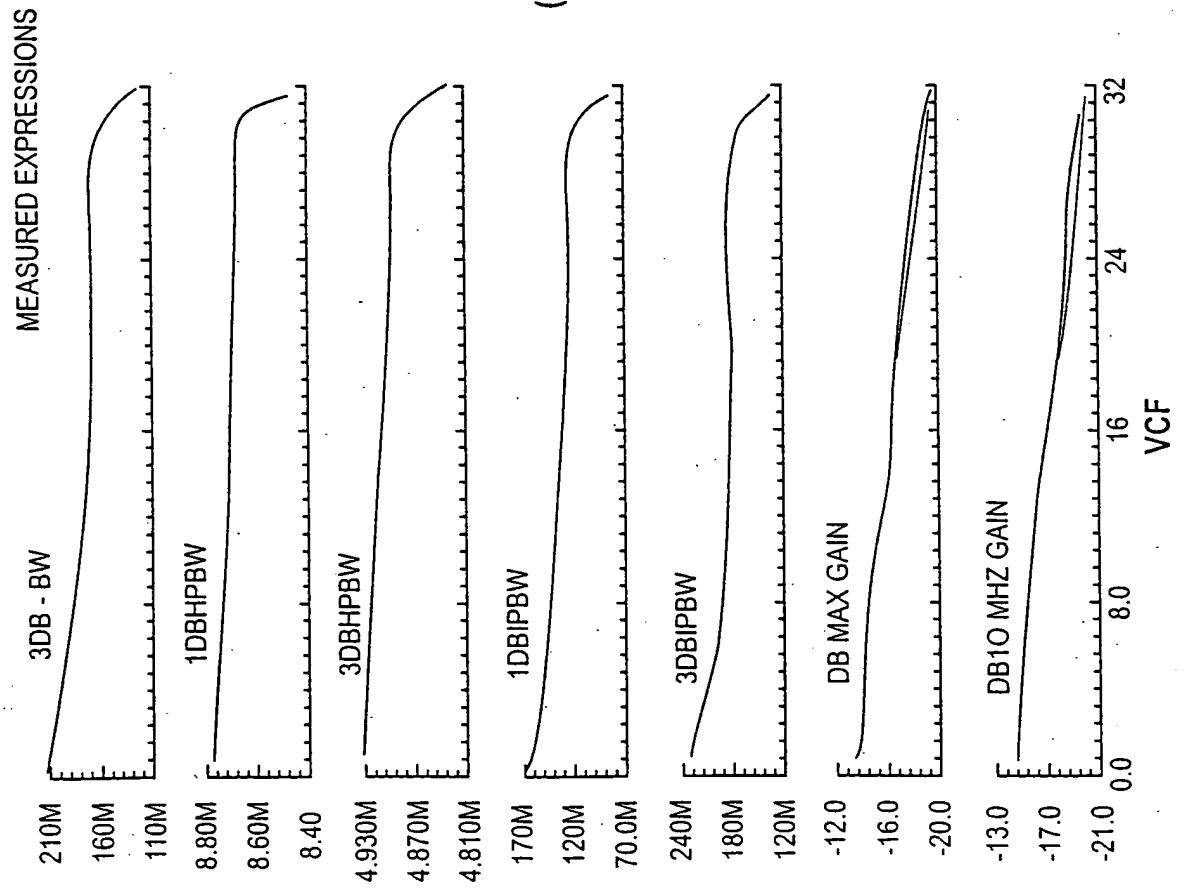
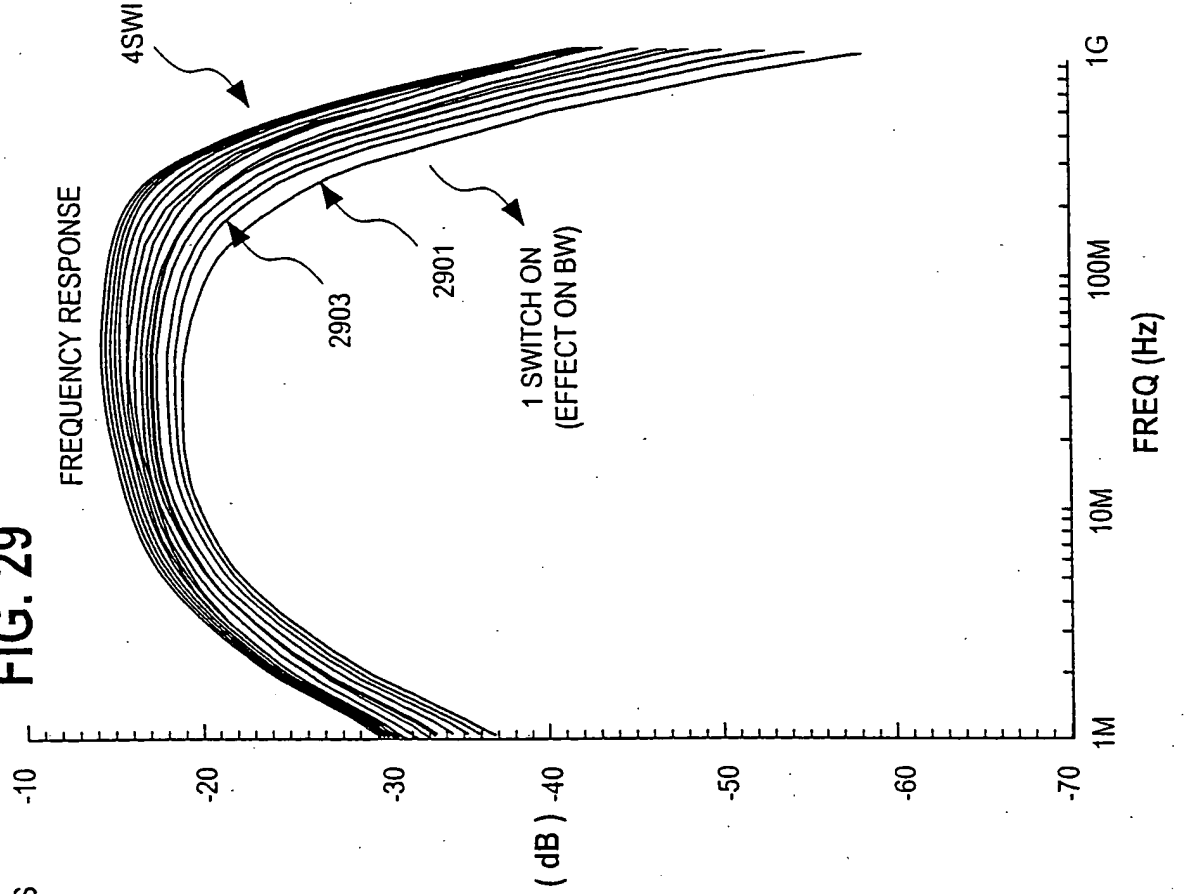


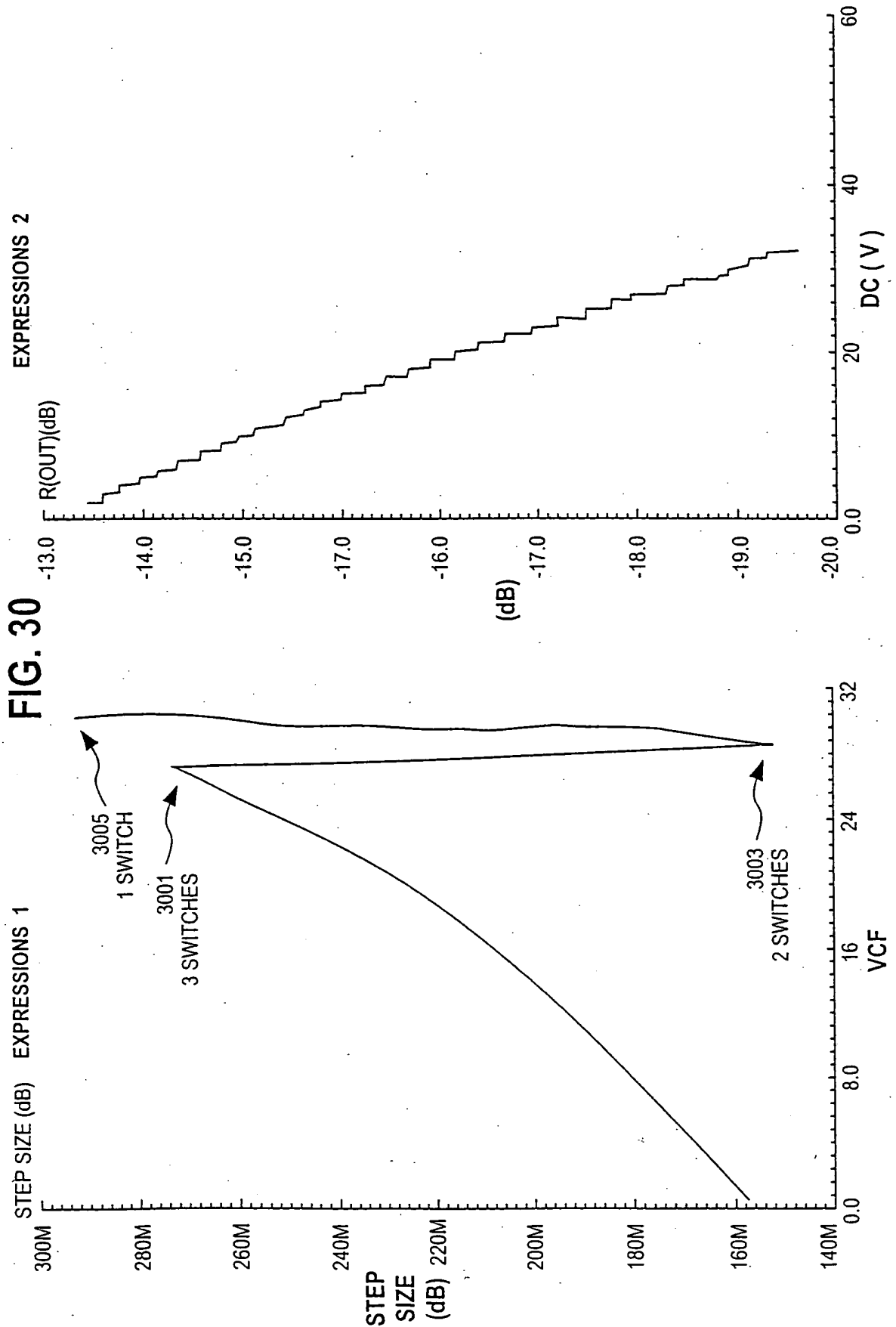
FIG. 28



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FIG. 29





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FIG. 31

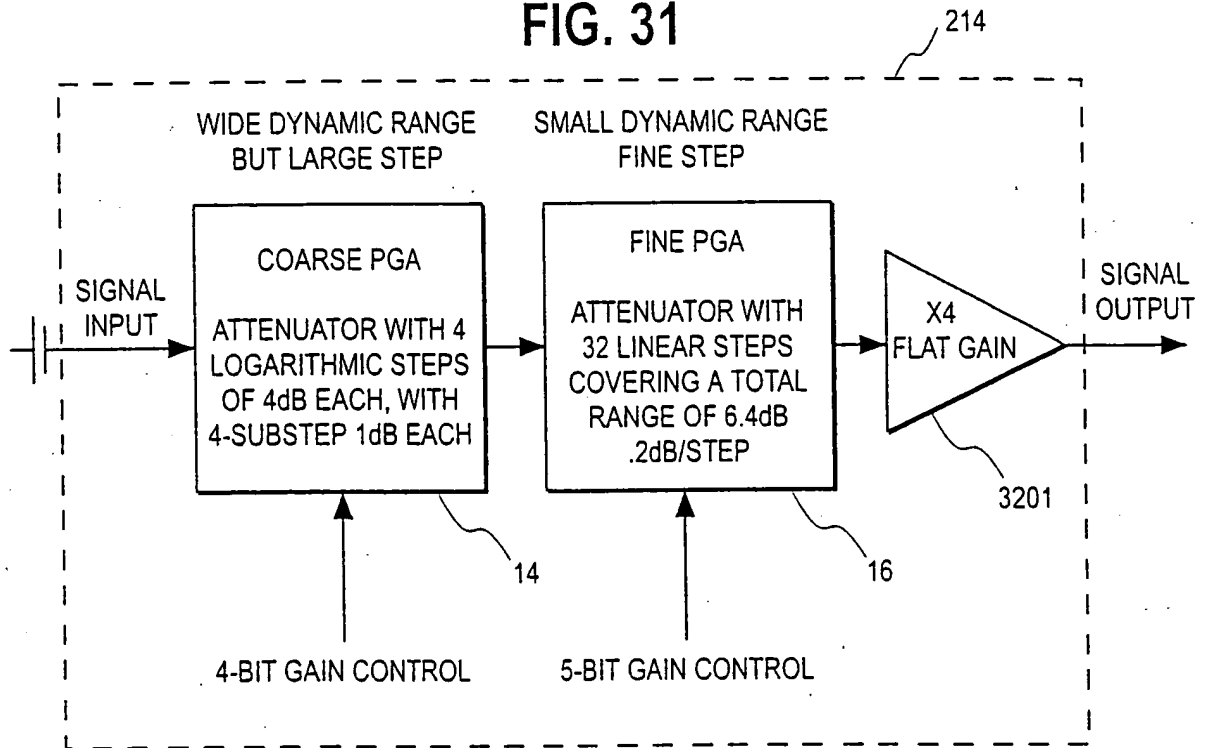


FIG. 32

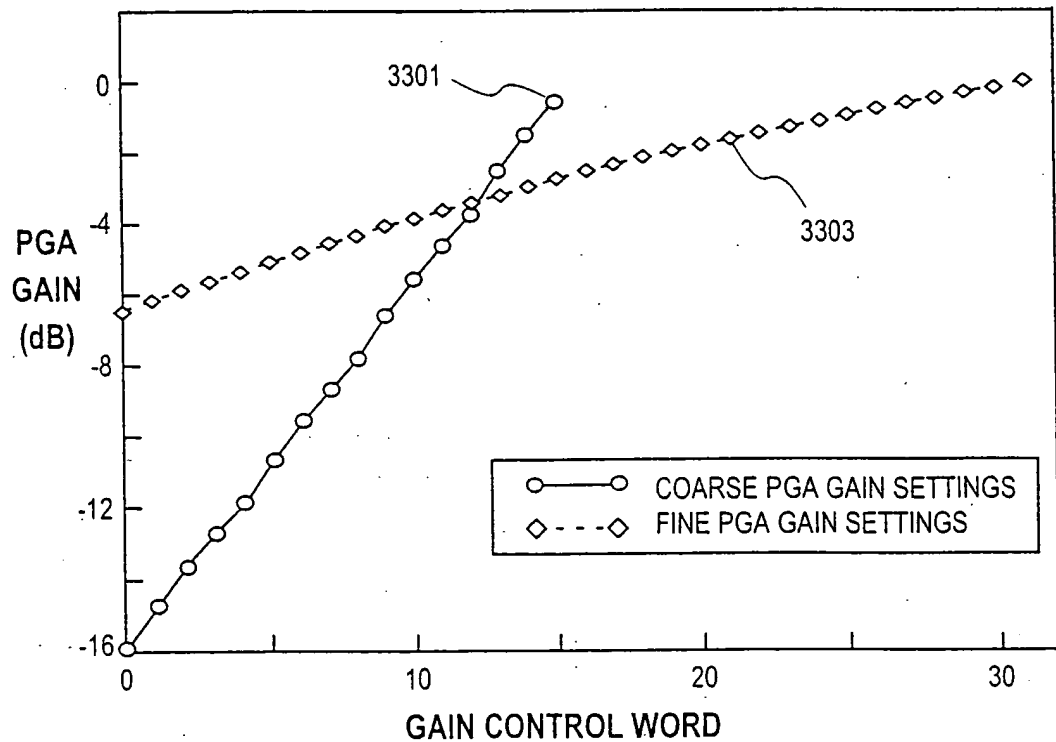
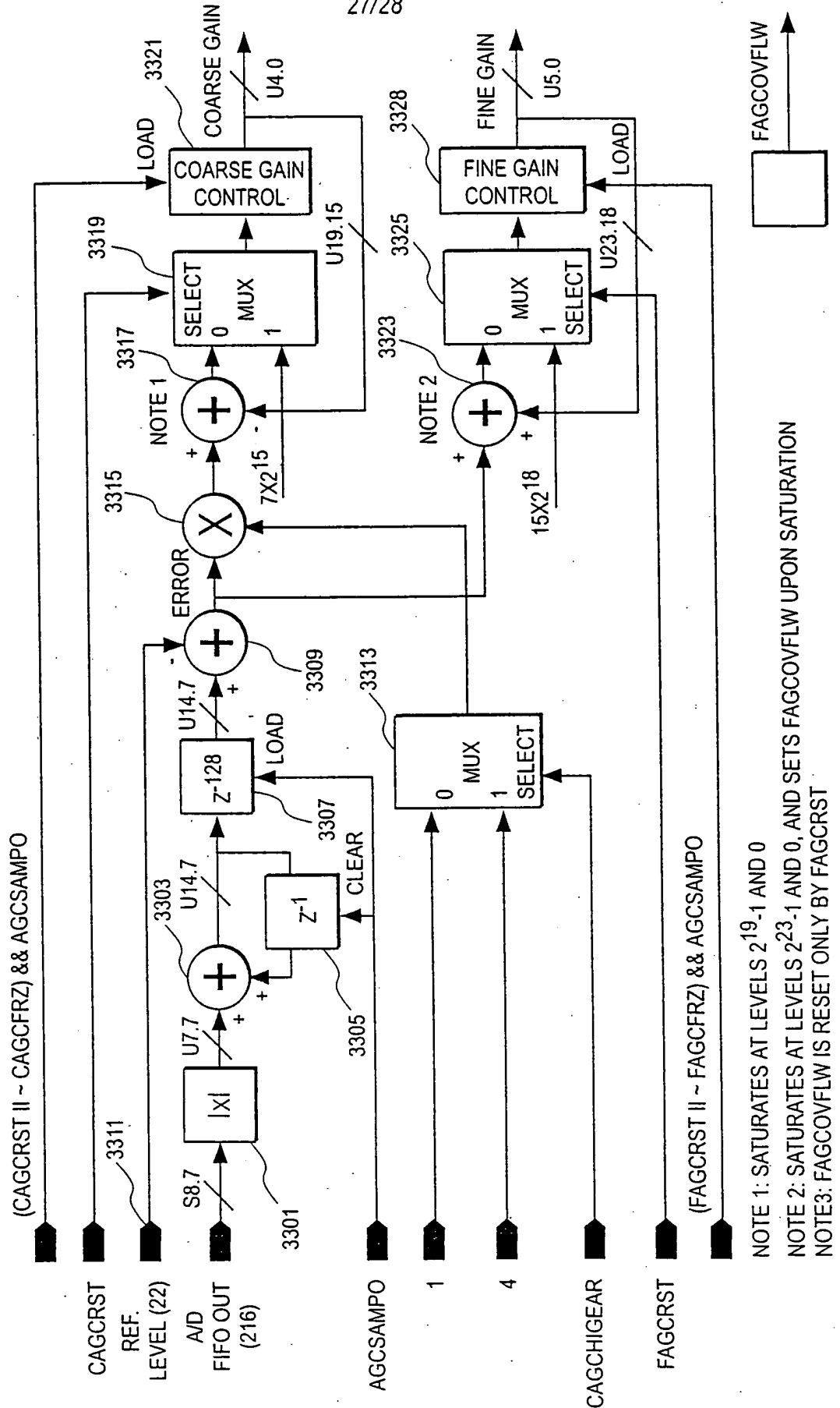


FIG. 33



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FIG. 34

CABLE LENGTH (m)	100 BASE- TX	GIGABIT, 100 OHM	GIGABIT, 85 OHM	GIGABIT, 115 OHM
0	3.691281	4.193192	4.193192	4.193192
20	3.806628	4.501316	4.362110	4.291369
40	3.877284	4.528136	4.457336	4.429949
60	3.894216	4.733644	4.695307	4.646305
80	4.055372	4.878569	4.847844	4.810019
100	4.225522	4.983545	4.991296	4.968900
120	4.357733	5.134131	5.194401	5.154263
140	4.556012	5.266919	5.380943	5.366309
160	4.764462	-	-	-

$$\begin{aligned} \text{TARGET } E\{IXI\} &= A/D \text{ CLIPPING LEVEL} \times (E\{IXI\}/\text{RMS})/(\text{PEAK}/\text{RMS}) \\ &= 127 \times 0.7979/5.2 = 20 \end{aligned}$$